

# PCI Express XpressRich Build History



Version	Build	Package Changes
2.1.0	131	<ul style="list-style-type: none"> <li>• Updated Core for compliance with PCI Express 2.0 specifications</li> </ul>
1.8.2	130	<ul style="list-style-type: none"> <li>• Implemented additional functionality for Bridge ports.</li> </ul>
1.8.1	129	<ul style="list-style-type: none"> <li>• Updated Reference Manual (see Reference Manual: Document Change History for details)</li> <li>• RTL bug corrections (see code changes listed in the Revision History (revision_history.pdf))</li> </ul>
1.8.0	127	<ul style="list-style-type: none"> <li>• Corrected bug in Verilog source code: a bit was missing from a Generic parameter (G_TAG_NUM).</li> <li>• Corrected Wizard bug: initialization of Generics for the top instance were misplaced within the configuration file.</li> </ul>
1.8.0	126	<ul style="list-style-type: none"> <li>• Up to eight functions supported for Endpoint configurations</li> <li>• Added MSI-X Capabilities support</li> <li>• Updated Reference Manual (see Reference Manual: Document Change History for details) <ul style="list-style-type: none"> <li>• Added new signals</li> <li>• Modified the names of some existing signals</li> <li>• Modified the meaning of certain bits of some signals</li> <li>• Updated the Common Configuration Space Header description to include MSI-X and SSID / SSVID Capability registers</li> </ul> </li> </ul>
1.7.2	128	<ul style="list-style-type: none"> <li>• Unwanted VC's optimized out. For VHDL top level file should activate wanted VC's. By default all VC's are enabled:</li> </ul> <pre>G_IMPL_VC7 : integer := 1; .... G_IMPL_VC1 : integer := 1</pre> <p>For verilog by default only VC0 is enabled. For enabling VC's different than VC0, a -define should be used at synthesis and simulation environments.</p>
1.7.0	125	<ul style="list-style-type: none"> <li>• Updated wizard added to package</li> <li>• Added missing programming files</li> <li>• Documentation: Minor changes made to Getting Started manual</li> </ul>
1.7.0	124	<ul style="list-style-type: none"> <li>• Documentation: Getting Started manual updated</li> <li>• Documentation: Reference Manual updated</li> <li>• Documentation: code changes listed in the Revision History (revision_history.pdf)</li> <li>• Switch support added to Core</li> <li>• New Reference Design</li> <li>• PLDA PCIe Testbench added to package</li> </ul>

Version	Build	Package Changes
1.6.0	123	<ul style="list-style-type: none"><li>• Documentation: New version of the Getting Started manual for the FPGA Source package</li><li>• Documentation: Replaced Reference Design with description of the EZ module</li><li>• Package structure modified</li></ul>
1.6.0	122	<ul style="list-style-type: none"><li>• Documentation: Introduction of <i>PCI Express Base Specification Revision 1.1</i> changes</li><li>• Documentation: new screenshots of Wizard appear in the Getting Started guide</li></ul>
1.5.2	121	<ul style="list-style-type: none"><li>• Restructuring of package</li><li>• New Switch signals added to the <i>Reference Manual</i>.</li><li>• New synthesis examples added to <i>Getting Started: ASIC</i>.</li><li>• New simulation environment that uses the NSys BFM</li><li>• Documentation: Addition of Switch signals to the Reference Manual</li><li>• Documentation: Significant update of the Getting Started guide</li><li>• Added support for ASPM L1</li></ul>
1.5.1	118	<ul style="list-style-type: none"><li>• Help buttons added to Wizard windows</li><li>• Documentation: minor updates of Reference Manual</li><li>• Documentation: new screenshots of Wizard appear in the Getting Started guide</li></ul>
1.5.1	117	<ul style="list-style-type: none"><li>• Product name changed from “PCI Express Core” to “PCI Express Expert Core”</li><li>• Documentation: minor updates of Reference Manual</li></ul>
1.5.0	116	<ul style="list-style-type: none"><li>• None</li></ul>
1.5.0	115	<ul style="list-style-type: none"><li>• The wizard now permits you to configure the Slot Register Space</li><li>• Documentation: update of Reference Manual</li><li>• Documentation: update of Getting Started; addition of Slot Register Space window description</li></ul>
1.4.2	114	<ul style="list-style-type: none"><li>• Documentation: update of Reference Manual</li></ul>
1.4.2	113	<ul style="list-style-type: none"><li>• Documentation: update of Reference Manual</li></ul>
1.4.1	112	<ul style="list-style-type: none"><li>• Configuration wizard update</li><li>• Documentation: update of Reference Manual. New sections describing ASPM and TLP poisoning</li><li>• Documentation: update of Getting Started</li><li>• Documentation: Split Getting Started into 3 similar documents for ASIC, Altera FPGA, and Xilinx FPGA</li></ul>
1.4	111	<ul style="list-style-type: none"><li>• Documentation: update of Reference Manual</li><li>• Bug fix of the Master block in the Reference Design</li></ul>
1.3.3	110	<ul style="list-style-type: none"><li>• Documentation: update of Reference Manual</li></ul>
1.3.2	109	<ul style="list-style-type: none"><li>• New Reference Design for the x1 125MHz Core</li><li>• New Reference Design for the x4 250MHz Core</li><li>• Configuration wizard update</li><li>• Documentation: update of Reference Manual</li><li>• Documentation: update of Getting Started guide</li></ul>
1.3.1	108	<ul style="list-style-type: none"><li>• DC Compiler script upgrade</li></ul>
1.3.1	107	<ul style="list-style-type: none"><li>• NCSim script upgrade</li><li>• Modelsim script upgrade</li></ul>
1.3.1	106	<ul style="list-style-type: none"><li>• Configuration wizard update</li><li>• Update of Reference Design</li><li>• Documentation: update of Reference Manual</li><li>• Documentation: update of Getting Started guide</li></ul>

Version	Build	Package Changes
1.3	105	<ul style="list-style-type: none"> <li>• New wizard to simplify configuration of the Core</li> <li>• Documentation: update of Reference Manual</li> <li>• Documentation: update of Getting Started guide</li> <li>• Reference Design update</li> </ul>
1.2.1	103	
1.2	102	<ul style="list-style-type: none"> <li>• Documentation: update of Reference Manual including details relating to the “k_XXX” configuration signals.</li> <li>• Documentation: update of Getting Started guide</li> </ul>
1.2	101	<ul style="list-style-type: none"> <li>• Updated source code to include x8 design files (ASIC packages only)</li> </ul>
1.2	100	<ul style="list-style-type: none"> <li>• New wizard to simplify configuration of the Core</li> <li>• Documentation: update of Getting Started guide</li> <li>• Documentation: update of Reference Manual</li> </ul>
1.1.2	101	<ul style="list-style-type: none"> <li>• IP Wizard bug fix</li> <li>• Simulation support for NCSim</li> </ul>
1.1.2	100	<ul style="list-style-type: none"> <li>• Test libraries updated for ModelSim</li> <li>• Test libraries added for NCSim</li> <li>• Documentation: update of Getting Started guide</li> <li>• Documentation: update of Reference Manual</li> </ul>
1.1.1	100	<ul style="list-style-type: none"> <li>• Documentation: update of Getting Started guide</li> <li>• Documentation: update of Reference Manual</li> </ul>
1.1.0	100	<ul style="list-style-type: none"> <li>• Documentation: First release of Getting Started guide</li> <li>• Documentation: First release of Reference Manual</li> </ul>
1.0.0	100	