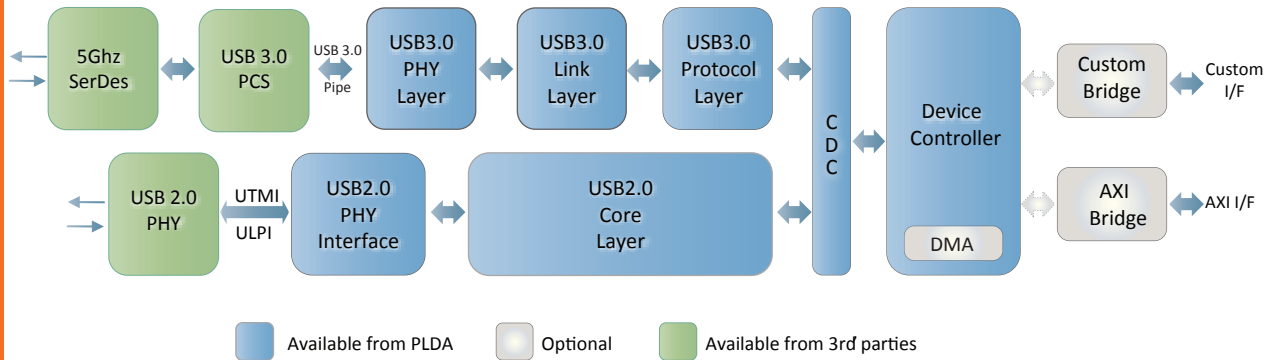


USB Device IP For ASIC and SoC Design



USB 3.0 solution from the industry's leading provider of interconnect IP



Features

- Full USB Specification support:
 - Full power management support (U1, U2, U3)
 - Up to 16 IN and OUT endpoints
 - Supports Isochronous and Interrupt endpoints
 - Supports Bulk Stream
 - Supports all USB 3.0 device notifications
- Flexible support for USB 2.0, allows custom USB 2.0 implementations
 - PLDA USB 2.0 Core Layer
 - Proprietary USB 2.0 implementations
- USB PIPE interface to PHY (8-, 16-, or 32-bit)
- Configurable Core frequency and variable datapath (32-, 64-, 128-bit)
- Available with AMBA AXI user interface
 - Custom user interfaces available for additional flexibility
- Flexible clocking scheme enables asynchronous user design operation
- Configurable buffer sizes allows optimization of system performance and resource utilization
- Embedded DMA engine

Reference Design

PCI Express® to Mass Storage:

Implements a USB-based mass storage device by connecting PLDA's USB 3.0 Device IP to RAM memory.

The reference design includes CPU emulator to perform IP configuration functions. When connected to a USB 3.0 host port, the operating system initializes the design as a mass storage device. I/O read/write can be issued to the device to access the memory content, e.g. through O/S-provided file transfer functions.

Benefits

- 16 years of experience supporting interface IP - over 1000 designs in working silicon
- Prototyping solutions for both Altera and Xilinx FPGA
- Dedicated technical support, directly from the IP designers, with fast and accurate turnaround
- Free testbench provided
- Customization services available to quickly and reliably fit specific customer requirements
- Customizable RTL allows customer to synthesize-out unnecessary logic, providing a lower gate count and small footprint

Deliverables

- IP synthesizable RTL source code in Verilog (ASIC)
- Configuration Wizard
- IP simulation models
- Testbench Verilog source code
- ASIC Synthesis scripts
- Reference designs

Free Evaluation

- License and Eval versions share same deliverables
- Includes Testbench
- Trial period includes full technical support

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