



PCI-X & PCI Core

Getting Started: ASIC

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Getting Started

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Product Status

The information in this document is final content pertaining to the PLDA PCI-X & PCI Core.

Web Address

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Preface

About this document

Intended Audience

This document has been written for design managers, system engineers, and designers of ASICs who are evaluating or using the PLDA PCI-X & PCI IP Core.

Scope

This document provides information to enable designers to integrate the PLDA PCI-X & PCI IP into their design flow as quickly as possible (installing, customizing, integrating, and simulating the Core). Accompanied by the *Reference Manual*, these two documents comprise all of the documentation for the PLDA PCI-X & PCI Core.

Typographical Conventions

<i>italic</i>	Highlights important notes or publications
bold	Highlights interface elements.
COURIER NEW	DENOTES TEXT USED IN A CODE EXAMPLE OR A SIGNAL.

Additional Reading

This section lists additional resources from PLDA and third-parties.

PLDA periodically updates its documentation. Please contact PLDA at support@plda.com or check the Web site at <http://www.plda.com> for current versions.

PLDA Publications

Please refer to the following documents for further information:

- *PCI-X & PCI Reference Manual*: The *Reference Manual* provides the complete functional description of the PLDA PCI-X & PCI Core.
- *PCI-X & PCI Testbench Reference Manual*: This document describes PLDA's PCI-X & PCI Testbench.
- *Build History*: The *Build History* lists changes made in each version and build of the Core.

Other Publications

Please refer to the following documents for information on specification standards:

- *PCI-X Addendum to the PCI Local Bus Specification , revision 2.0a - PCI SIG, July 2003*
- *PCI Local Bus Specification , revision 3.0 - PCI Special Interest Group, February 2004*
- *PCI Compliance Checklist , revision 3.0 - PCI Special Interest Group, March 2004*
- *PCI Mobile Design Guide, revision 1.1 - PCI Special Interest Group, December 1998*
- *PCI Bus Power Management Interface, revision 1.2 - PCI SIG, March 2004*
- *CompactPCI Hot Swap Specification , revision 1.0 - PICMG, August 1998*
- *MiniPCI Specification , revision 1.0 - PCI Special Interest Group, October 1999*
- *PC Cards Standard , release 8.0 - PCMCIA Association, April 2001*

Feedback and Contact Information

Feedback about this Document

PLDA welcomes comments and suggestions about this documentation. Please contact PLDA Technical Support and provide the following information:

- the title of the document
- the page number to which your comments refer
- a description of your comments

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If you don't have a PLDA account, contact http://www.plda.com/support_enquiry.php.

Chapter 1 Before you Start...

1.1 System Requirements

To install the PCI-X & PCI package, you need:

- **Memory:** 1 Gb of RAM or greater
- **Operating System:** Windows 2000/XP/Vista or any UNIX/Linux platform supporting Java
- **Hard Disk:** 1 GB for Core installation and component design

1.2 EDA Tools Requirements

The following table describes EDA Tools Requirements unique to Windows, unique to Unix/Linux, and common to both operating systems.

Table 1: EDA Tools Requirements

Windows 2000/XP/Vista	Unix/Linux
	NCSim version 5.50 p004
ModelSim PE or SE 6.1d or later	

1.3 Package Features

The PCI-X & PCI Core is available for Windows or Unix/Linux in one of the following packages:

- ASIC Source
 - **Windows:** *pcixpci_vXXX_bYYY_asic_source.zip*
 - **Unix / Linux:** *pcixpci_vXXX_bYYY_asic_source.tar.gz*
- ASIC Board/Eval
 - **Windows:** *pcixpci_vXXX_bYYY_asic_board_eval.zip*
 - **Unix / Linux:** *pcixpci_vXXX_bYYY_asic_board_eval.tar.gz*

1.4 Installing the Package

1.4.1 Windows 2000, XP, or Vista

To install the Core package, unzip ***pcixpci_vXXX_bYYY_ZZZ.zip*** to your hard drive; “XXX” is the Core version number, “YYY” is the build number, and “ZZZ” is the supported technology.

1.4.2 UNIX/Linux Platform

1. Open a shell and set the working directory to the directory where the Core package has been download from the PLDA web site.
2. Unzip the tar.gz file using unzip software, such as WinRAR or 7-Zip.
3. Create an empty directory.
4. At the prompt, type:

```
tar -xzf pcixpci_vXXX_bYYY_ZZZ.tar.gz -C <your directory path>
```

“XXX” is the Core version number, “YYY” is the build number, and “ZZZ” is the supported technology.

1.5 Exploring the Installed Files

Table 2: Directory structure for the installed package

<ul style="list-style-type: none"> • core <ul style="list-style-type: none"> • pci • source <ul style="list-style-type: none"> • vhdl/vlog: RTL clear-text core source code • simulation <ul style="list-style-type: none"> • Modelsim <ul style="list-style-type: none"> • vhdl/vlog: pre-compiled simulation library • ncsim <ul style="list-style-type: none"> • vhdl/vlog: compiled simulation library • VCS <ul style="list-style-type: none"> • vhdl/vlog: compiled simulation library
<ul style="list-style-type: none"> • documentation <ul style="list-style-type: none"> build_history.pdf revision_history.pdf getting_started.pdf reference_manual.pdf Testbench_reference_manual.pdf • appnotes <ul style="list-style-type: none"> • application notes and sample source code
<ul style="list-style-type: none"> • testsuite <ul style="list-style-type: none"> • Testsuite environment
<ul style="list-style-type: none"> • ref_design <ul style="list-style-type: none"> • Reference Design for simulation
<ul style="list-style-type: none"> • software <ul style="list-style-type: none"> • plda_api: Application Programming Interface files • tools_source: C++ examples of PLDA tools • windows: PCI drivers and PLDA tools executables
<ul style="list-style-type: none"> • Testbench: PLDA PCI-X & PCI Testbench <ul style="list-style-type: none"> • pci • source <ul style="list-style-type: none"> • vhdl/vlog: RTL clear-text core source code • simulation <ul style="list-style-type: none"> • Modelsim <ul style="list-style-type: none"> • vhdl/vlog: pre-compiled simulation library • ncsim <ul style="list-style-type: none"> • vhdl/vlog: compiled simulation library • VCS <ul style="list-style-type: none"> • vhdl/vlog: compiled simulation library
<ul style="list-style-type: none"> • wizard: TxRx interface wizard provided for creating a top-level instance of the Core.

Chapter 2 Frontend Design

2.1 Creating a Parameterized Instance of the Core

You can create a customized core using the PLDA PCI-X & PCI Wizard. The Wizard creates a VHDL or Verilog wrapper that instantiates the core with custom parameter values, input ports and output ports. To launch the Wizard:

- **Windows:** Browse to the /wizard directory and run the run_wizard_pcixpci.bat batch file to launch the Wizard GUI.
- **Unix/Linux:** Open a terminal window and type: /bin/sh run_wizard_pcixpci.sh (located in the ../wizard installation directory)

Once launched, the Wizard prompts you to enter a name for the wrapper, or to browse and select a wrapper that has already been created to edit.

The first page of the Wizard enables you to define the main characteristics of the Core. Subsequent pages enable you to customize the Core.

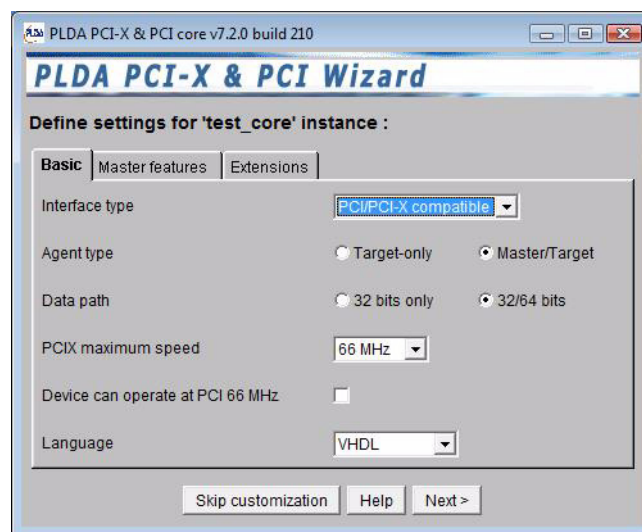


Figure 1: PCI-X & PCI Wizard

Click the **<Help>** button anytime for detailed information about each option.

2.2 You can also use the PLDA PCI-X & PCI Wizard **Simulation with ModelSim**

The Core package contains all the elements required for VHDL or Verilog simulation with Mentor ModelSim version 6.1 or later. Functional models for the Core and the Testbench are provided as pre-compiled libraries. Follow these steps to create and simulate a design:

1. Start ModelSim and create a new project.
2. Add source files to the project, making sure to include the Wizard-generated instance of the Core.
3. Type the following commands at the Modelsim prompt to map and update Core and Testbench libraries:

VHDL

```
vmap pcixpcitestb_lib
    install_path/Testbench/pci/modelsim/vhdl/pcixpcitestb_lib
vcom -force_refresh -work pcixpcitestb_lib

vmap pcixpcicore_lib
    install_path/core/pci/modelsim/vhdl/pcixpcicore_lib
vcom -force_refresh -work pcixpcicore_lib
```

Verilog

```
vmap pcixpcitestb_lib
  install_path/Testbench/pci/modelsim/vlog/pcixpcitestb_lib
vlog -force_refresh -work pcixpcitestb_lib

vmap pcixpcicore_lib
  install_path/core/pci/modelsim/vlog/pcixpcicore_lib
vlog -force_refresh -work pcixpcicore_lib
```

It is now possible to simulate any custom instance of the PCI-X & PCI Core and backend logic with the Testbench. Refer to the *PCI-X & PCI Testbench Reference Manual* for more information.

2.3 Simulation with NCSim

The Core package contains all the elements required for VHDL or Verilog simulation with Cadence NCSim or Incisive Unified Simulator version 5.5p004 or later. You must build simulation libraries before you start simulation. To build simulation libraries:

1. Create and map the libraries named “pcixpcitestb_lib” and “pcixpcicore_lib”
2. Enter the following commands at the NCLaunch prompt to build the Core and Testbench libraries:

VHDL

```
ncvhdl -93 -work pcixpcicore_lib -update
  install_path/core/pci/ncsim/vhdl/pcixpcicore_lib.vhdp
ncvhdl -93 -work pcixpcitestb_lib -update
  install_path/Testbench/pci/ncsim/vhdl/pcixpcitestb_lib.vhdp
```

Verilog

```
ncvlog -work pcixpcicore_lib -update
  install_path/core/pci/ncsim/vlog/pcixpcicore_lib.vp
ncvlog -work pcixpcitestb_lib -update
  install_path/Testbench/pci/ncsim/vlog/pcixpcitestb_lib.vp
```

2.4 Timing Compliance

PCI & PCI-X specifications impose stringent timing requirements on PCI signals, as detailed in the table below:

Table 3: Timing compliance

	33MHz PCI	66MHz PCI	66MHz PCI-X	133MHz PCI-X
Tsu (set-up time to clock)	7ns*	3ns**	1.7ns	1.2ns
Tco (clock-to-output time)	11ns	6ns	3.8ns	3.8ns
Th (hold time)	0ns	0ns	0.5ns	0.5ns
Thz (OE-to-output time)	28ns	14ns	7ns	7ns

* 10ns for point-to-point signals (REQ#, GNT#)

** 5ns for point-to-point signals (REQ#, GNT#)

The PLDA PCI-X & PCI Wizard creates a *Tcl* project setup script which generates all necessary constraints when launched in Quartus II (see [Section 2.2](#) for details).

66MHz PCI designs require additional constraints, such as logic placement, to be added to conform to PCI timing

requirements. PLDA provides custom optimization services for 66MHz PCI designs; these are described in the Core License Agreement.

