



# SW\_HSI Daughter Card

## Reference Manual

Version 1.1 June 2008  
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## SW\_HSI

### Reference Manual

#### About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA SW\_HSI daughter card. Prior knowledge of PCI Express is assumed.

#### Document Change History

| Date           | Board Version | Change  |
|----------------|---------------|---|
| June 2007      | 1.1           | <ul style="list-style-type: none"><li>• Updated pin assignments, card photo and mechanical description</li><li>• Added sections on clock selection and cabling driver configuration</li></ul> |
| September 2007 | 1.1           | <ul style="list-style-type: none"><li>• Updated to include XpressLXT support</li></ul>  |
| January 2007   | 1.0           | <ul style="list-style-type: none"><li>• First Release</li></ul>   |

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#### Contact information

##### Corporate Headquarters

PLDA  
Parc club du golf - Bât. 11a  
Rue Guilibert  
13856 Aix-en-Provence Cedex 3 - France

Tel: USA +1 408 273 4528 - International +33 442 393 600

Fax: +33 442 394 902

##### Sales

For sales questions, please contact [sales@plda.com](mailto:sales@plda.com).

##### Technical Support

For technical support questions, please contact [support@plda.com](mailto:support@plda.com).

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## Chapter 1 Purpose of the SW\_HSI

The SW\_HSI (Switch on High Speed Interface) daughter card extends the latest generation of PLDA boards by adding switch capabilities using:

- two x1 lane PCI Express female connectors
- one x4 lane on a x8 PCI Express female connector
- one x1 link on a x4 PCI Express cable connector

**Note:** The x8 PCI Express female connector is not available with the XpressFX, XpressAGX, or XpressV5LC mother boards.

Compatible boards include:

- XpressFX100 version 2.0
- XpressGXII version 1.1
- XpressGen2GX version 1.0
- XpressLXT version 2.0
- XpressGen2V5 version 1.0
- XpressAGX version 1.0
- XpressV5LC version 1.0

You can download the Reference Manuals for these boards from [www.plda.com](http://www.plda.com).

## Chapter 2 SW\_HSI Architecture

### 2.1 SW\_HSI Components

The following figure shows the SW\_HSI daughter card:

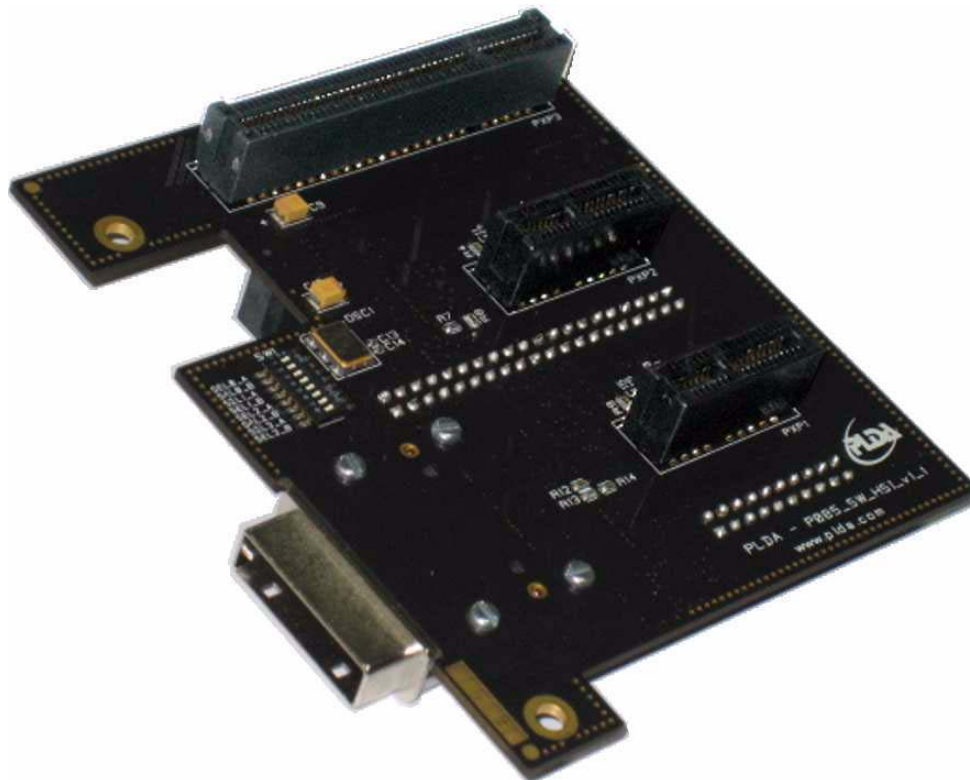


Figure 1: SW\_HSI layout

## 2.2 Block Diagram of the SW\_HSI

The following figure illustrates internal SW\_HSI connections:

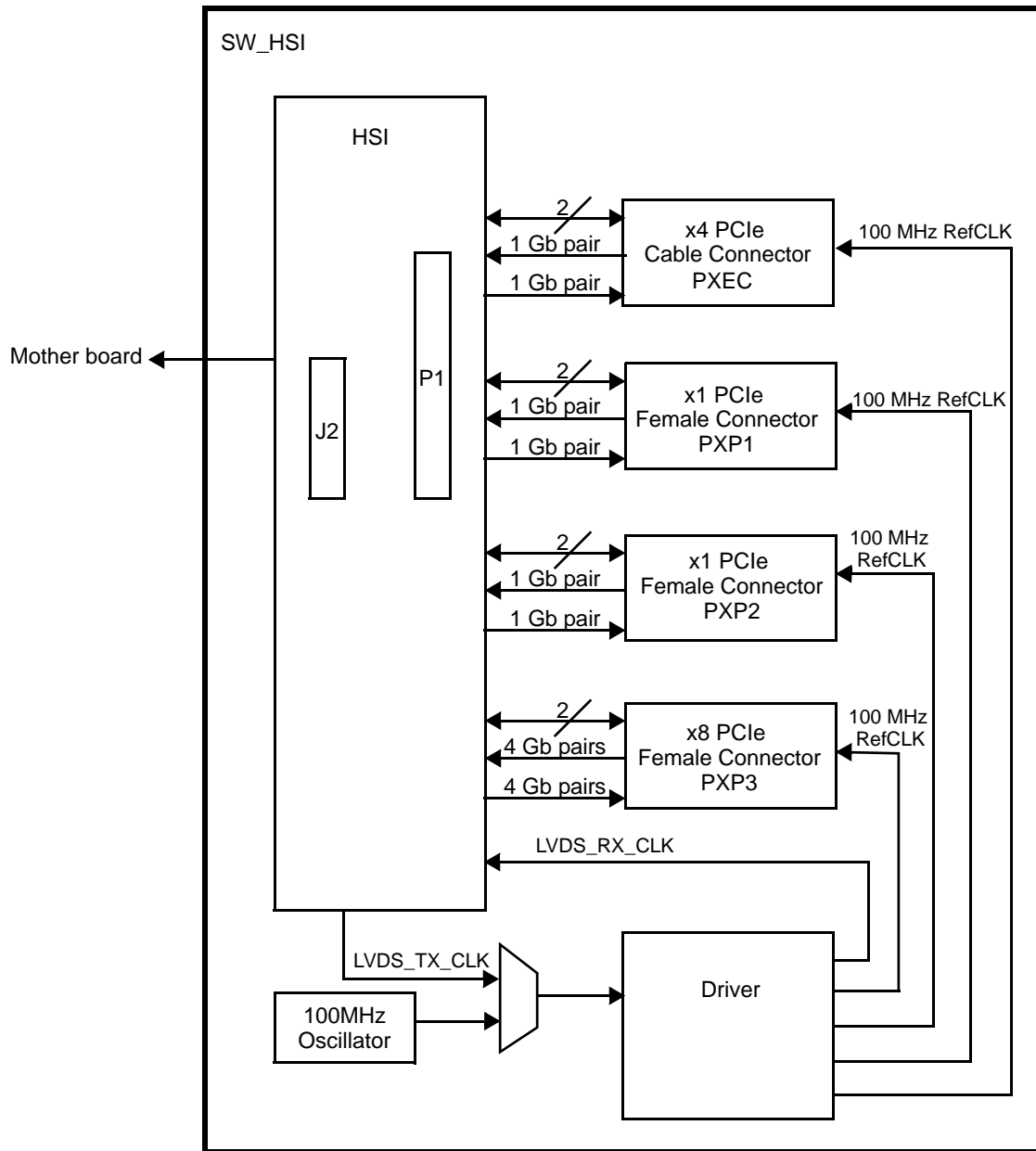


Figure 2: SW\_HSI block diagram

## 2.3 Mechanical Description of the SW\_HSI

The following figure illustrates the mechanical architecture of the SW\_HSI:

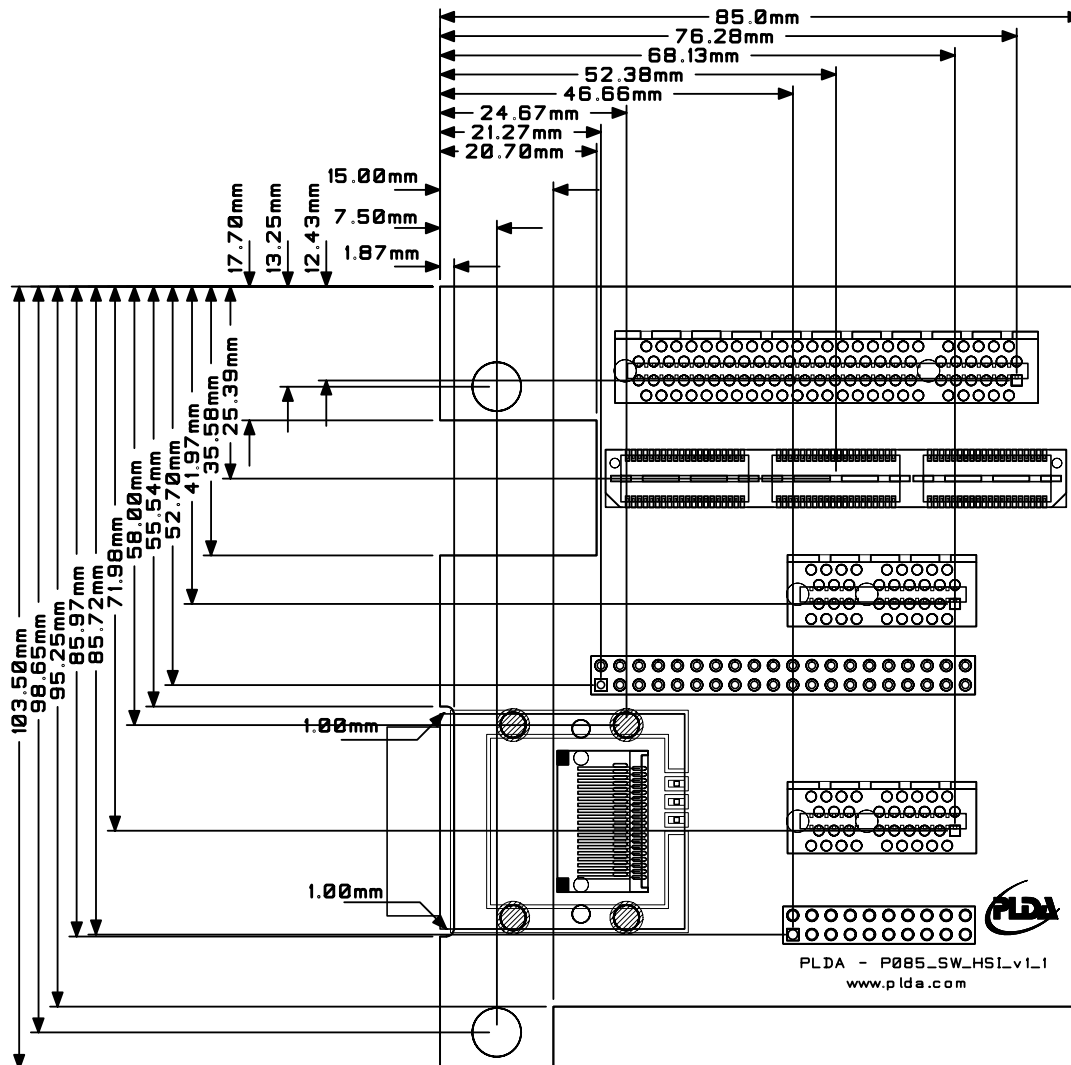


Figure 3: SW\_HSI mechanical architecture

The diagram below shows a transparent view of the SW\_HSI to illustrate the components on the underside of the card. The height of the components is shown in millimetres:

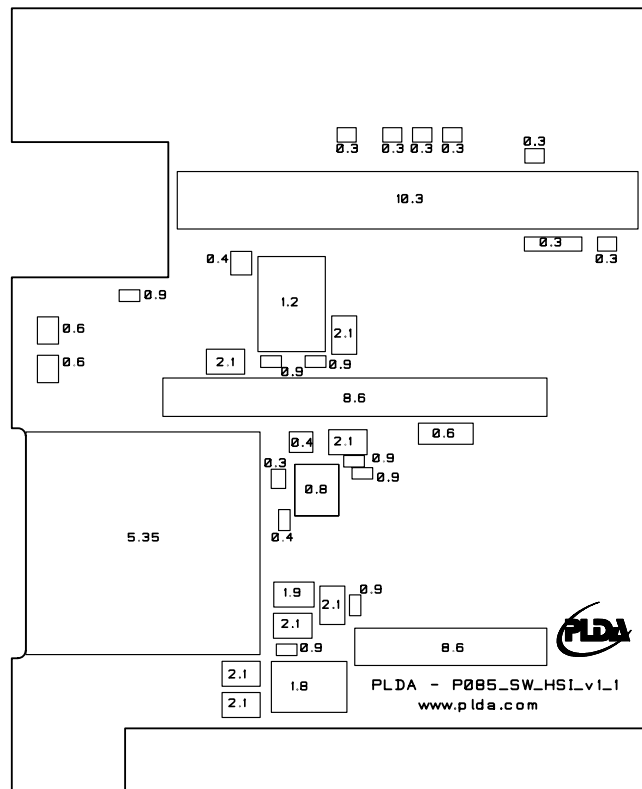


Figure 4: Height of components on the underside

## Chapter 3 SW\_HSI Resources

The following tables list pin assignments between the SW\_HSI and the corresponding pin assignments on compatible mother boards.

### 3.1 Pin Assignments for PXEC PCIe Cabling Connector

The PXEC is a x4 cable connector that enables a x1 PCI Express link:

Table 1: Pin assignments for PCIe cabling connector

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressGX2 XpressGen2GX | XpressAGX | XpressV5LC |
|------------------|-------------|---------------------|----------|------------------------|------------------------|-----------|------------|
| J1-3             | cPETp0      | Gbit_Tx0p           | A25      | B10                    | C4                     | V4        | B2         |
| J1-4             | cPERp0      | Gbit_Rx0p           | A28      | A9                     | C1                     | V1        | C1         |
| J1-5             | cPETn0      | Gbit_Tx0n           | A26      | B9                     | C5                     | V5        | C2         |
| J1-6             | cPERn0      | Gbit_Rx0n           | A29      | A8                     | C2                     | V2        | D1         |
| P2-1             | cWAKE       | Matrix_IO13         | T10      | E17                    | D11                    | A12       | Y4         |
| P2-3             | cPRSNT      | Matrix_IO14         | T9       | G17                    | B10                    | C11       | W4         |
| P2-5             | cPERST      | Matrix_IO15         | U6       | F16                    | D12                    | C10       | T8         |
| P2-7             | cPWRON      | Matrix_IO16         | R6       | D16                    | B12                    | B14       | T5         |

### 3.2 Pin Assignments for PXP1 PCIe x1 Connector

Table 2: Pin assignments for PXP1

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressGX2 XpressGen2GX | XpressAGX | XpressV5LC |
|------------------|-------------|---------------------|----------|------------------------|------------------------|-----------|------------|
| J1-15            | f1PETp0     | Gbit_Tx2p           | A15      | B4                     | E4                     | AD4       | H2         |
| J1-16            | f1PERp0     | Gbit_Rx2p           | A18      | A3                     | E1                     | AB1       | J1         |
| J1-17            | f1PETn0     | Gbit_Tx2n           | A14      | B3                     | E5                     | AD5       | J2         |
| J1-18            | f1PERn0     | Gbit_Rx2n           | A17      | A2                     | E2                     | AB2       | K1         |
| P2-9             | f1PERST     | Matrix_IO17         | P6       | D15                    | B13                    | D10       | R5         |
| P2-15            | f1PRSNT     | Matrix_IO20         | K4       | A15                    | A14                    | D11       | L8         |

### 3.3 Pin Assignments for PXP2 PCIe x1 Connector

Table 3: Pin assignments for PXP2

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressGX2 XpressGen2GX | XpressAGX | XpressV5LC |
|------------------|-------------|---------------------|----------|------------------------|------------------------|-----------|------------|
| J1-21            | f2PETp0     | Gbit_Tx3p           | A13      | E2                     | G4                     | AF4       | N2         |
| J1-22            | f2PERp0     | Gbit_Rx3p           | A10      | D1                     | G1                     | AD1       | M1         |
| J1-23            | f2PETn0     | Gbit_Tx3n           | A12      | D2                     | G5                     | AF5       | M2         |
| J1-24            | f2PERn0     | Gbit_Rx3n           | A9       | C1                     | G2                     | AD2       | L1         |
| P2-11            | f2PERST     | Matrix_IO18         | N8       | C15                    | D13                    | C13       | R7         |
| P2-13            | f2PRSNT     | Matrix_IO19         | P9       | B15                    | D15                    | D14       | P6         |

### 3.4 Pin Assignments for PXP3 PCIe x8 Connector

The PXP3 is a x8 female connector that enables a x4 PCI Express link:

Table 4: Pin assignments for PXP3

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressGX2 XpressGen2GX | XpressAGX | XpressV5LC |
|------------------|-------------|---------------------|----------|------------------------|------------------------|-----------|------------|
| J1-85            | f3PETp0     | Gbit_Tx4p           | --       | F2                     | L4                     | --        | --         |
| J1-86            | f3PERp0     | Gbit_Rx4p           | --       | G1                     | L1                     | --        | --         |
| J1-87            | f3PETn0     | Gbit_Tx4n           | --       | G2                     | L5                     | --        | --         |
| J1-88            | f3PERn0     | Gbit_Rx4n           | --       | H1                     | L2                     | --        | --         |
| J1-91            | f3PETp1     | Gbit_Tx5p           | --       | L2                     | J4                     | --        | --         |
| J1-92            | f3PERp1     | Gbit_Rx5p           | --       | K1                     | J1                     | --        | --         |
| J1-93            | f3PETn1     | Gbit_Tx5n           | --       | K2                     | J5                     | --        | --         |
| J1-94            | f3PERn1     | Gbit_Rx5n           | --       | J1                     | J2                     | --        | --         |
| J1-97            | f3PETp2     | Gbit_Tx6p           | --       | M2                     | N4                     | --        | --         |
| J1-98            | f3PERp2     | Gbit_Rx6p           | --       | N1                     | N1                     | --        | --         |
| J1-99            | f3PETn2     | Gbit_Tx6n           | --       | N2                     | N5                     | --        | --         |
| J1-100           | f3PERn2     | Gbit_Rx6n           | --       | P1                     | N2                     | --        | --         |
| J1-103           | f3PETp3     | Gbit_Tx7p           | --       | U2                     | R4                     | --        | --         |
| J1-104           | f3PERp3     | Gbit_Rx7p           | --       | T1                     | R1                     | --        | --         |
| J1-105           | f3PETn3     | Gbit_Tx7n           | --       | T2                     | R5                     | --        | --         |
| J1-106           | f3PERn3     | Gbit_Rx7n           | --       | R1                     | R2                     | --        | --         |
| P2-17            | f3PERST     | Matrix_IO21         | --       | B16                    | A15                    | --        | --         |
| P2-21            | f3PRSNT     | Matrix_IO22         | --       | B17                    | B16                    | --        | --         |

**Note:** The PXP3 connector is not available with the XpressFX, XpressAGX, or XpressV5LC boards.

### 3.5 Pin Assignments for PLL Configuration

The SW\_HSI uses the PLL ICS9DB803DGLF to generate all 100 MHz Reference Clocks:

**Table 5: Pin assignments for PLL configuration - Xilinx-based boards**

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressV5LC | PLL I/O  |
|------------------|-------------|---------------------|----------|------------------------|------------|--|
| P2-4             | PLL_LOCKED  | Matrix_IO32         | U7       | D17                    | U5         | PLL output:<br>high when PLL locked                    |
| P2-33            | BYPASS_PLL  | Matrix_IO28         | F5       | D20                    | H6         | PLL input:<br>0 = Bypass mode, 1= PLL mode             |
| P2-35            | PLL_HIGH_BW | Matrix_IO29         | G5       | E21                    | G4         | PLL input: PLL BW selection:<br>0 = High BW, 1= Low BW |
| P2-23            | CLK_OE_0    | Matrix_IO23         | H4       | G18                    | L5         | PLL Input: 0 = High-Z,<br>1= PEXEC clock active        |
| P2-25            | CLK_OE_1    | Matrix_IO24         | F4       | F18                    | L7         | PLL input:<br>0 = High-Z, 1= PXP1 clock active         |
| P2-27            | CLK_OE_2    | Matrix_IO25         | H5       | F19                    | K5         | PLL input:<br>0 = High-Z, 1= PXP2 clock active         |
| P2-29            | CLK_OE_3    | Matrix_IO26         | P10      | E19                    | J5         | PLL input:<br>0 = High-Z, 1= PXP3 clock active         |
| P2-31            | CLK_OE_4    | Matrix_IO27         | N10      | D19                    | J6         | PLL input:<br>LVDS_Rx_CLK clock active = 1             |

**Table 6: Pin assignments for PLL configuration - Altera-based boards**

| SW_HSI J1/P2 pin | Signal name | Mother board signal | XpressGX2 XpressGen2GX | XpressAGX | PLL I/O  |
|------------------|-------------|---------------------|------------------------|-----------|--|
| P2-4             | PLL_LOCKED  | Matrix_IO32         | C11                    | A13       | PLL output:<br>high when PLL locked                    |
| P2-33            | BYPASS_PLL  | Matrix_IO28         | C18                    | J10       | PLL input:<br>0 = Bypass mode, 1= PLL mode             |
| P2-35            | PLL_HIGH_BW | Matrix_IO29         | D18                    | K12       | PLL input: PLL BW selection:<br>0 = High BW, 1= Low BW |
| P2-23            | CLK_OE_0    | Matrix_IO23         | A16                    | G12       | PLL Input: 0 = High-Z,<br>1= PEXEC clock active        |
| P2-25            | CLK_OE_1    | Matrix_IO24         | F17                    | G13       | PLL input:<br>0 = High-Z, 1= PXP1 clock active         |
| P2-27            | CLK_OE_2    | Matrix_IO25         | D17                    | G10       | PLL input:<br>0 = High-Z, 1= PXP2 clock active         |
| P2-29            | CLK_OE_3    | Matrix_IO26         | A17                    | H13       | PLL input:<br>0 = High-Z, 1= PXP3 clock active         |
| P2-31            | CLK_OE_4    | Matrix_IO27         | A18                    | H11       | PLL input:<br>LVDS_Rx_CLK clock active = 1             |

## 3.6 Pin Assignments for Clock Synchronization

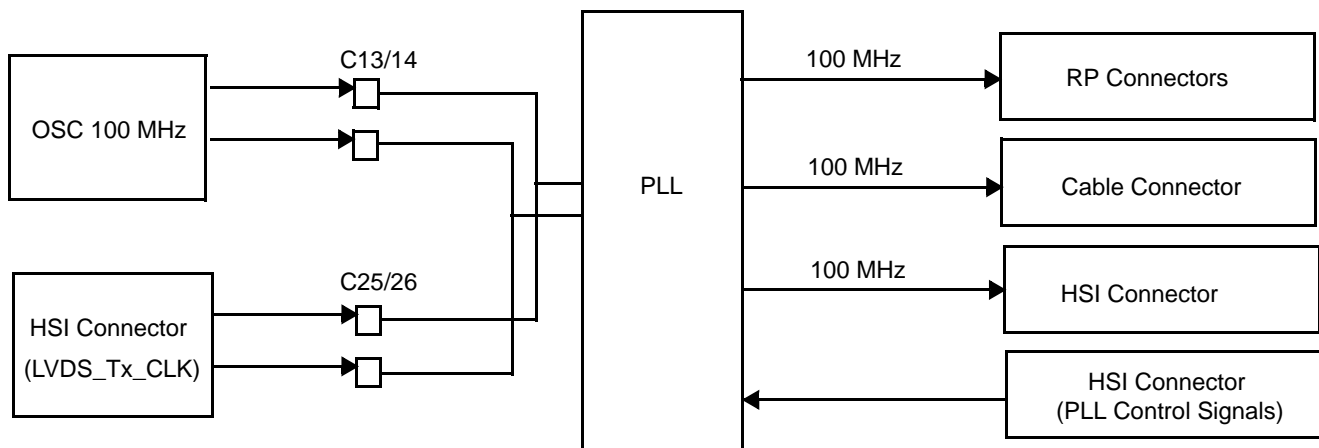
Table 7: Pin assignments for clock synchronization

| SW_HSI J1/P2 pin | Signal name  | Mother board signal | XpressFX | XpressLXT XpressGen2V5 | XpressGXII XpressGen2GX | XpressAGX | XpressV5LC |
|------------------|--------------|---------------------|----------|------------------------|-------------------------|-----------|------------|
| J1-27            | LVDS_Tx_CLKp | LVDS_Tx_CLKp        | K23      | *                      | W32                     | T19       | *          |
| J1-28            | LVDS_Rx_CLKp | LVDS_Rx_CLKp        | G22      | E4                     | F7                      | Y1        | D4         |
| J1-29            | LVDS_Tx_CLKn | LVDS_Tx_CLKn        | L23      | *                      | Y31                     | U19       | *          |
| J1-30            | LVDS_Rx_CLKn | LVDS_Rx_CLKn        | H22      | D4                     | F8                      | Y2        | D3         |

**Note:** \* On XpressLXT, XpressGen2V5, and XpressV5LC, the LVDS\_Tx\_CLKp/n signal is driven by the PCIe 100MHz reference clock. See the Reference Manual for each of these boards for more information.

## 3.7 Reference Clock Source Selection

You can generate the 100 MHz reference clock either from the local oscillator or from the mother board, as shown below: .



- If you want to generate the Reference Clock using the local oscillator (which is the default configuration), verify that C13/C14 is mounted and C25/C26 is not mounted.
- If you want to generate the Reference Clock using LVDS\_Tx\_CLK (the mother board clock), mount C25/26 and remove C13/14.

### 3.8 PCIe Cabling Driver Configuration

The following diagram illustrates the configuration of the PCIe cabling drivers (on the solder side of the card):

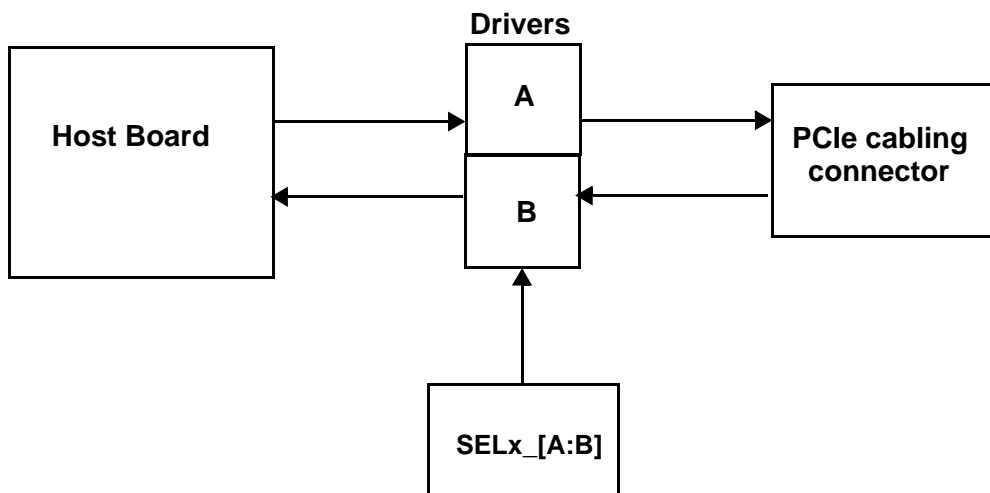


Figure 5: PCIe cabling drivers configuration

You can configure the PCIe cabling drivers to upgrade signal integrity using the card's switches, as shown below:



Figure 6: Photograph of the user switches

The table below shows how to configure output swing control using the switch SEL2:

Table 8: Output swing control

| SEL2_[A:B] | Swing |
|------------|-------|
| 0          | 1x    |
| 1          | 1.2x  |

The table below shows how to configure output de-emphasis adjustment using the switch SEL3:

Table 9: Output de-emphasis adjustment

| SEL3_[A:B] | De-emphasis |
|------------|-------------|
| 0          | 0dB         |
| 1          | -3.5dB      |

The table below shows how to configure equalizer selection using the switches SEL0 and SEL1:

**Table 10: Equalizer selection**

| SEL0 [A:B] | SEL1 [A:B] | Compliance Channel     |
|------------|------------|------------------------|
| 0          | 0          | No equalization        |
| 0          | 1          | [0:2.5dB] @ 1.25 GHZ   |
| 1          | 0          | [2.5:4.5dB] @ 1.25 GHZ |
| 1          | 1          | [4.5:6.5dB] @ 1.25 GHZ |