



RP_HSI Daughter Card

Reference Manual

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RP_HSI

Reference Manual

About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA RP_HSI daughter card. Prior knowledge of PCI Express is assumed.

Document Change History

Date	Card Version	Change
May 2008	1.1	• Updated to include new compatible mother boards
April 2008	1.1	• First documentation release

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Table of Contents

Chapter 1	Purpose of the RP_HSI	4
Chapter 2	RP_HSI Architecture	5
2.1	RP_HSI Components	5
2.2	Block Diagram of the RP_HSI	5
2.3	Mechanical Description of the RP_HSI	6
Chapter 3	RP_HSI Resources	7

Chapter 1 Purpose of the RP_HSI

The RP_HSI daughter card extends the latest generation of PLDA boards (boards that include Gigabit signals on the High-Speed Interface) by adding a x8 lane PCI Express female extension that enables:

- x1/x4/x8 Root Port applications
- PCI Express Switch applications

Compatible boards include:

- XpressLXT version 2.0
- XpressGen2V5 version 1.0
- XpressGXII version 1.1
- XpressGen2GX version 1.0

You can download the Reference Manuals for these boards from www.plda.com.

Note: The P2 connector required to mount the RP_HSI daughter card on compatible mother boards is included in the RP_HSI package.

Chapter 2 RP_HSI Architecture

2.1 RP_HSI Components

The following figure illustrates the component side of the RP_HSI daughter card:



Figure 1: RP_HSI layout

2.2 Block Diagram of the RP_HSI

The RP_HSI provides access to gigabit links from the mother board through the x8 lane PCI Express female connector. The following figure shows a block diagram of the RP_HSI:

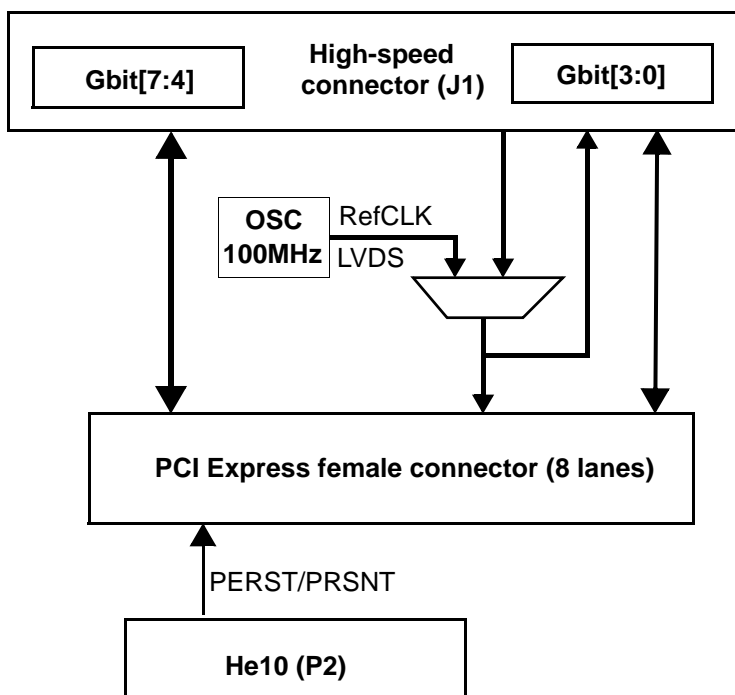


Figure 2: RP_HSI block diagram

2.3 Mechanical Description of the RP_HSI

The following figure illustrates the mechanical architecture of the RP_HSI daughter card:

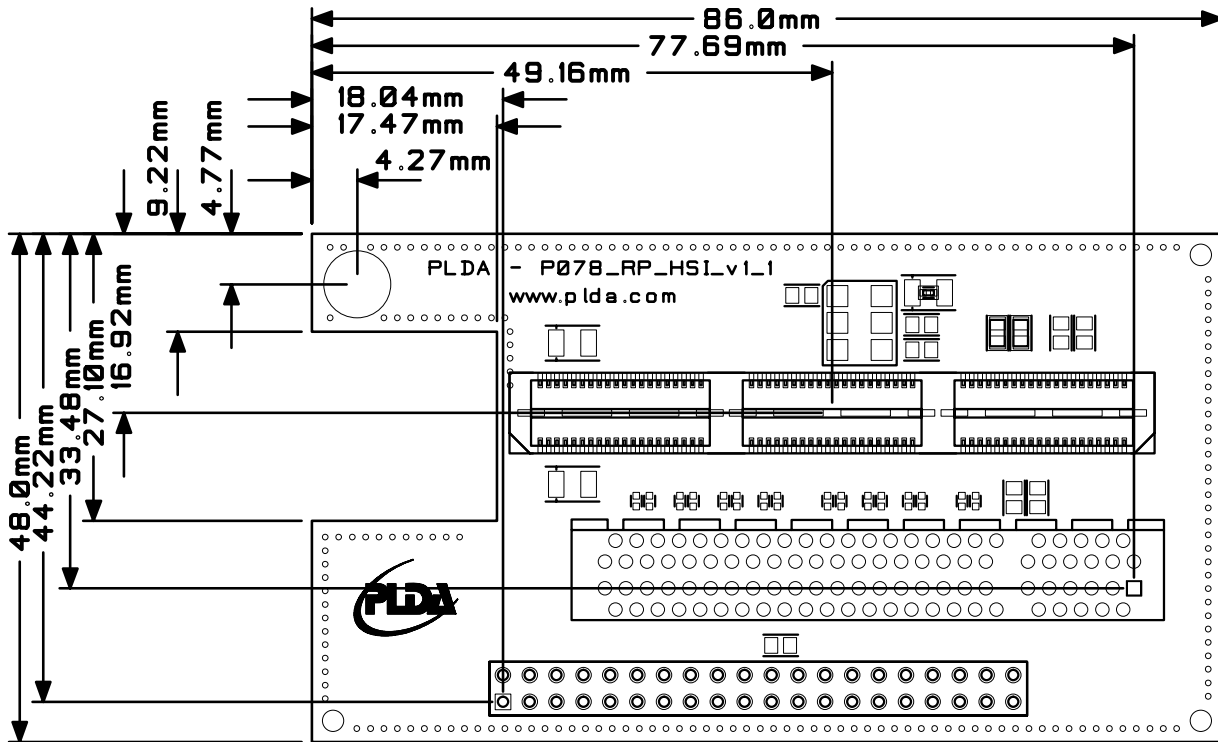


Figure 3: RP_HSI mechanical architecture

Chapter 3 RP_HSI Resources

The following table lists pin assignments between the RP_HSI and compatible mother boards:

Table 1: Pin assignments between the RP_HSI and the mother boards

RP_HSI signal	XpressLXT_V20 XpressGen2V5_V10	XpressGX2_V11 XpressGen2GX_V10
fPER0p/n	A9/A8	C1/C2
fPER1p/n	A6/A7	A3/A4
fPER2p/n	A3/A2	E1/E2
fPER3p/n	D1/C1	G1/G2
fPER4p/n	G1/H1	L1/L2
fPER5p/n	K1/J1	J1/J2
fPER6p/n	N1/P1	N1/N2
fPER7p/n	T1/R1	R1/R2
fPET0p/n	B10/B9	C4/C5
fPET1p/n	B5/B6	A6/A7
fPET2p/n	B4/B3	E4/E5
fPET3p/n	E2/D2	G4/G5
fPET4p/n	F2/G2	L4/L5
fPET5p/n	L2/K2	J4/J5
fPET6p/n	M2/N2	N4/N5
fPET7p/n	U2/T2	R4/R5
fPERST	C15	D13
fPRSNT	B15	D15
fREFCLK	From Mother board	From FPGA pins W32/Y31