



# KLINK\_Base Daughter Card

## Reference Manual

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## KLINK\_Base

### Reference Manual

#### About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA KLINK\_Base daughter board.

#### Document Change History

Date	Card Version	Change
May 2008	1.1	• Updated with new pin assignments and compatible mother boards
May 2006	1.0	• First release

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# Chapter 1 Purpose of the KLINK\_Base

The KLINK\_Base daughter card extends the latest generation of PLDA boards by adding base Camera Link™ resources. Camera Link™ is a standard communication interface for vision applications.

The devices implemented on the KLINK\_Base meet the base Camera Link standard, providing:

- 3 x 8-bit taps
- 4-bit synchronisation signals
- 4 command signals
- 1 bi-directional serial communication channel

These devices offer a 75MHz input data flow for an effective bandwidth of 225 MB/s.

Compatible boards include:

- XpressLXT version 2.0
- XpressGen2V5 version 1.0
- XpressGXII version 1.1
- XpressGen2GX version 1.0
- XpressAGX version 1.0
- XpressV5LC version 1.0
- XpressFX version 1.0
- PCI-X SYS V5 version 1.0
- PCI-X SYS2 version 1.0

You can download the Reference Manuals for these boards from [www.plda.com](http://www.plda.com).

## Chapter 2 KLINK\_Base Architecture

### 2.1 KLINK\_Base Components

The following figure shows the component side of the KLINK\_Base daughter card:

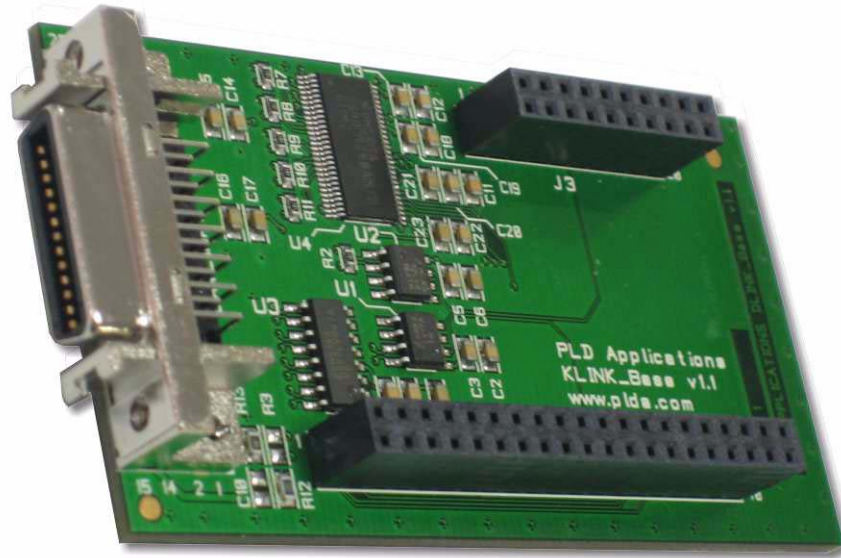


Figure 1: KLINK\_Base layout

## 2.2 KLINK\_Base Block Diagram

The KLINK\_Base provides access to the base Camera Link configuration and to all signals provided by Camera Link devices (up to 3 taps of 8 bits). The following figure shows a block diagram of the KLINK\_Base:

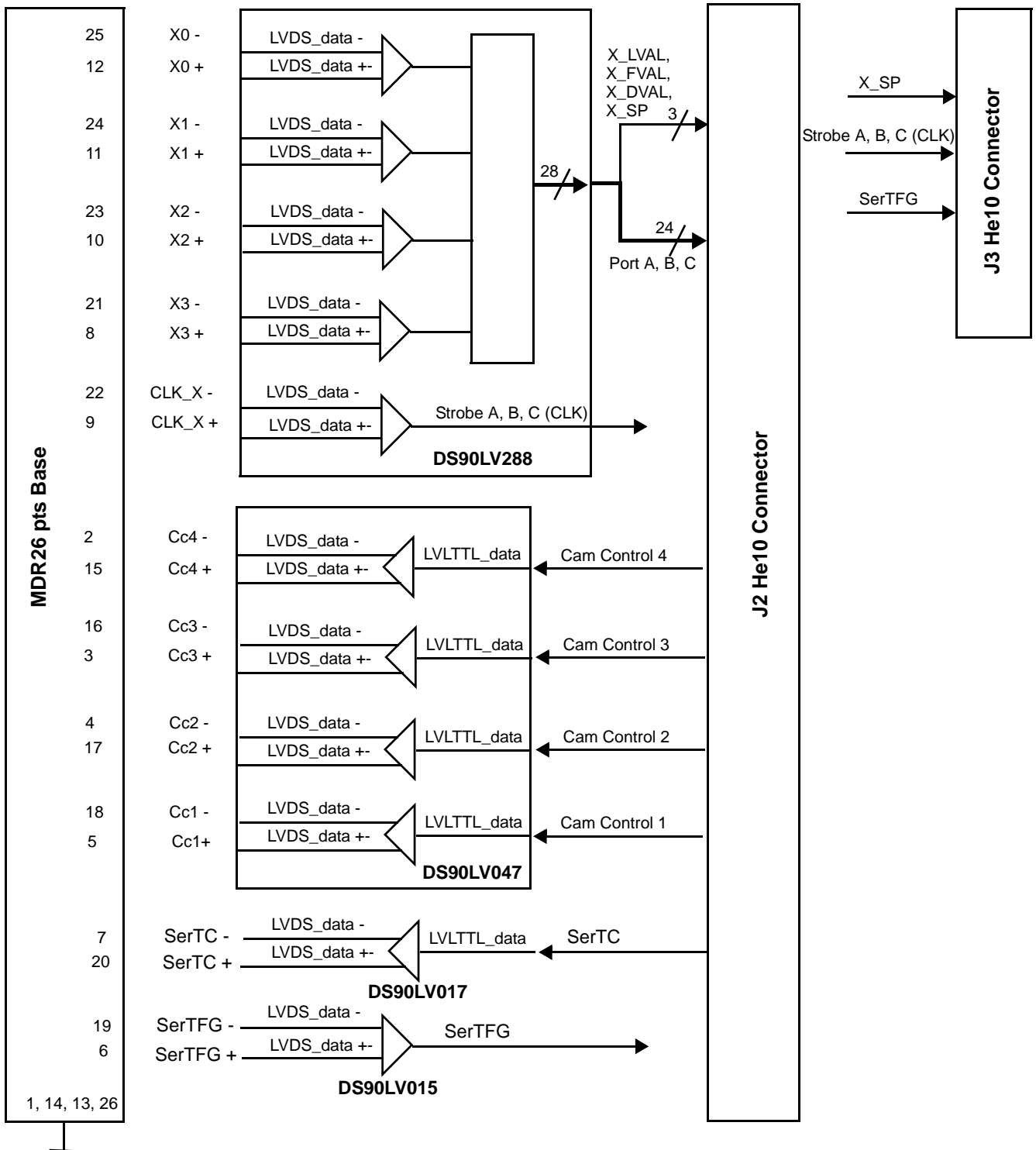


Figure 2: KLINK\_Base block diagram

### 2.3 Mechanical Description of the KLINK\_Base

The following figure illustrates the mechanical architecture of the KLINK\_Base daughter card:

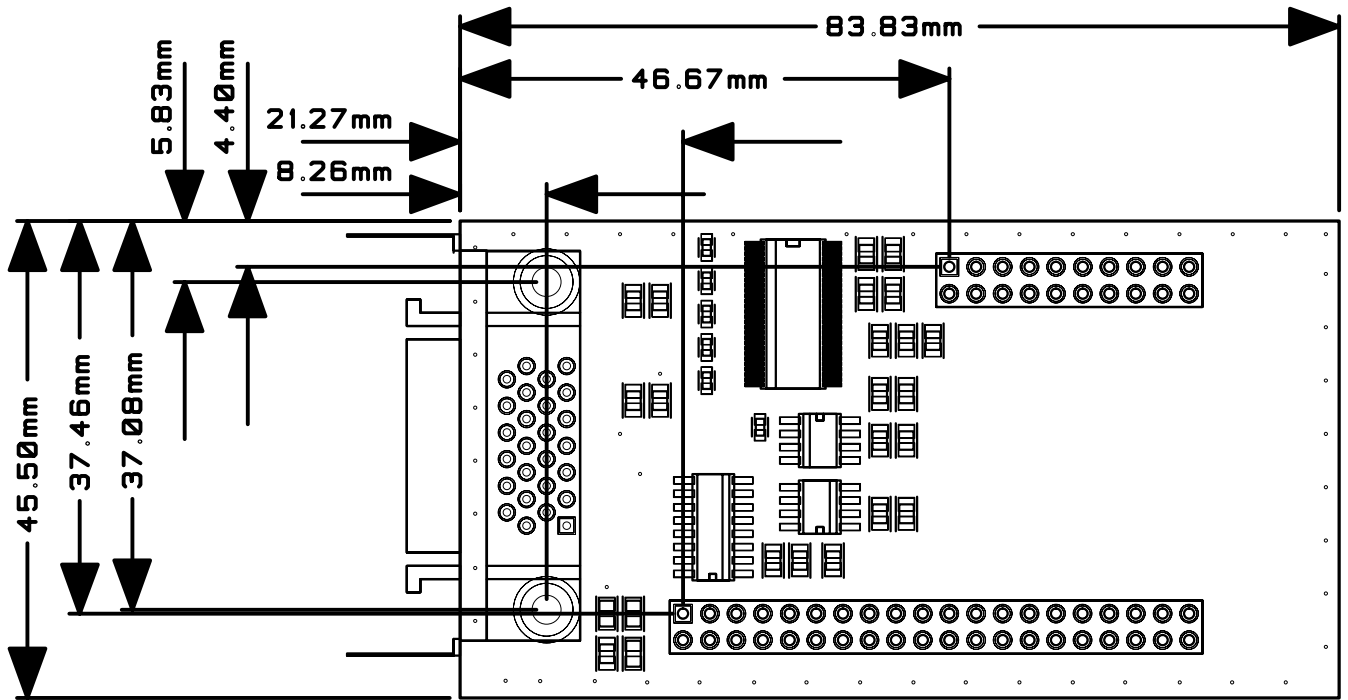


Figure 3: KLINK\_Base mechanical architecture

## Chapter 3 KLINK\_Base Resources

The following table lists pin assignments between the KLINK\_Base and the corresponding FPGA pin assignments on compatible Xilinx-based mother boards:

**Table 1: Pin assignments between KLINK\_Base and Xilinx-based mother boards**

Pin	Signal	Mother board signal	XpressFX	XpressLXT/ XpressGen2V5	XpressV5LC	PCI-X SYS V5
J2-1	port_A0	Matrix_IO13	T10	E17	Y4	F5
J2-3	XDVAL	Matrix_IO14	T9	G17	W4	H5
J2-4	port_A6	Matrix_IO32	U7	D17	U5	N6
J2-5	XLVAL	Matrix_IO15	U6	F16	T8	G6
J2-6	port_C5	Matrix_IO33	R8	E16	T7	M6
J2-7	port_C4	Matrix_IO16	R6	D16	T5	H6
J2-8	XFVAL	Matrix_IO34	R7	D14	R8	J6
J2-9	port_C2	Matrix_IO17	P6	D15	R5	G7
J2-10	port_C6	Matrix_IO35	P7	C14	R6	L6
J2-11	port_B5	Matrix_IO18	N8	C15	R7	J7
J2-12	port_C3	Matrix_IO36	L5	A14	P8	U7
J2-13	port_B3	Matrix_IO19	P9	B15	P6	K7
J2-14	port_B4	Matrix_IO37	K3	G20	K8	W7
J2-15	port_B2	Matrix_IO20	K4	A15	L8	M8
J2-16	Cam_Control1	Matrix_IO38	R9	G21	N8	V8
J2-17	port_B1	Matrix_IO21	J4	B16	N6	M9
J2-18	port_C0	Matrix_IO39	H3	F23	N7	Y8
J2-20	port_A1	Matrix_IO40	G3	C17	M6	Y9
J2-21	port_C1	Matrix_IO22	F3	B17	M7	N9
J2-23	port_A2	Matrix_IO23	H4	G18	L5	N8
J2-25	port_A3	Matrix_IO24	F4	F18	L7	R9
J2-27	port_C7	Matrix_IO25	H5	F19	K5	R8
J2-28	SerTC	Matrix_IO41	T11	E18	K6	Y10
J2-29	port_A4	Matrix_IO26	P10	E19	J5	T10
J2-31	Cam_Control4	Matrix_IO27	N10	D19	J6	T11
J2-32	port_A5	Matrix_IO42	N9	F20	H4	V10
J2-33	port_A7	Matrix_IO28	F5	D20	H6	T9
J2-35	port_B0	Matrix_IO29	G5	E21	G4	U9
J2-36	port_B6	Matrix_IO43	M10	E22	G5	U11
J2-37	Cam_Control3	Matrix_IO30	L6	D21	F5	U8
J2-38	port_B7	Matrix_IO44	L10	F21	G6	V11

Table 1: Pin assignments between KLINK\_Base and Xilinx-based mother boards

Pin	Signal	Mother board signal	XpressFX	XpressLXT/ XpressGen2V5	XpressV5LC	PCI-X SYS V5
J2-39	Cam_Control2	Matrix_IO31	M8	D22	K7	V9
J3-9	XSP	Local_OSC2	H17	U7	From OSC2	U6
J3-11	SerTFG	sc_clk0	L9	R8	AC17	R5
J3-13	STROBE_ABC	sc_clk1	L8	T8	AB14	U4

The following table lists pin assignments between the KLINK\_Base and the corresponding FPGA pin assignments on compatible Altera-based mother boards:

Table 2: Pin assignments between KLINK\_Base and Altera-based mother boards

Pin	Signal	Mother board signal name	XpressGXII/ XpressGen2GX	Xpress AGX	PCI-X SYS2
J2-1	port_A0	Matrix_IO13	D11	A12	AE12
J2-3	XDVAL	Matrix_IO14	B10	C11	AD12
J2-4	port_A6	Matrix_IO32	C11	A13	AE11
J2-5	XLVAL	Matrix_IO15	D12	C10	AJ10
J2-6	port_C5	Matrix_IO33	C12	B13	AG10
J2-7	port_C4	Matrix_IO16	B12	B14	AD18
J2-8	XFVAL	Matrix_IO34	A12	C12	AC18
J2-9	port_C2	Matrix_IO17	B13	D10	AH9
J2-10	port_C6	Matrix_IO35	C13	C14	AG9
J2-11	port_B5	Matrix_IO18	D13	C13	N23
J2-12	port_C3	Matrix_IO36	C14	D12	AH8
J2-13	port_B3	Matrix_IO19	D15	D14	AH7
J2-14	port_B4	Matrix_IO37	C15	D13	AJ6
J2-15	port_B2	Matrix_IO20	A14	D11	M23
J2-16	Cam_Control1	Matrix_IO38	B15	E14	AH6
J2-17	port_B1	Matrix_IO21	A15	E13	AJ5
J2-18	port_C0	Matrix_IO39	D16	E11	AH5
J2-20	port_A1	Matrix_IO40	C16	F13	AG8
J2-21	port_C1	Matrix_IO22	B16	E10	AF10
J2-23	port_A2	Matrix_IO23	A16	G12	M22
J2-25	port_A3	Matrix_IO24	F17	G13	AE10
J2-27	port_C7	Matrix_IO25	D17	G10	AD11
J2-28	SerTC	Matrix_IO41	C17	G9	AD10
J2-29	port_A4	Matrix_IO26	A17	H13	AC11

Table 2: Pin assignments between KLINK\_Base and Altera-based mother boards

Pin	Signal	Mother board signal name	XpressGXII/ XpressGen2GX	Xpress AGX	PCI-X SYS2
J2-31	Cam_Control4	Matrix_IO27	A18	H11	AB11
J2-32	port_A5	Matrix_IO42	B18	J11	AC12
J2-33	port_A7	Matrix_IO28	C18	J10	AB12
J2-35	port_B0	Matrix_IO29	D18	K12	AA22
J2-36	port_B6	Matrix_IO43	F18	K13	Y22
J2-37	Cam_Control3	Matrix_IO30	C19	K11	U22
J2-38	port_B7	Matrix_IO44	D19	L12	V23
J2-39	Cam_Control2	Matrix_IO31	F19	K10	U23
J3-9	XSP	Local_OSC2	B21	From OSC3	From OS2
J3-11	SerTFG	sc_clk0	G18	L13	AJ15
J3-13	STROBE_ABC	sc_clk1	G10	F15	AM17

## Chapter 4 Installation Examples

**Note:** The 40-pts J2 and 20-pts J3 HE10 connectors required to mount the KLINK\_Base daughter card on compatible mother boards are included in the KLINK\_Base package.

### 4.1 Mounting the KLINK\_Base on the XpressGXII

The following figure shows the KLINK\_Base daughter card mounted on the XpressGXII:

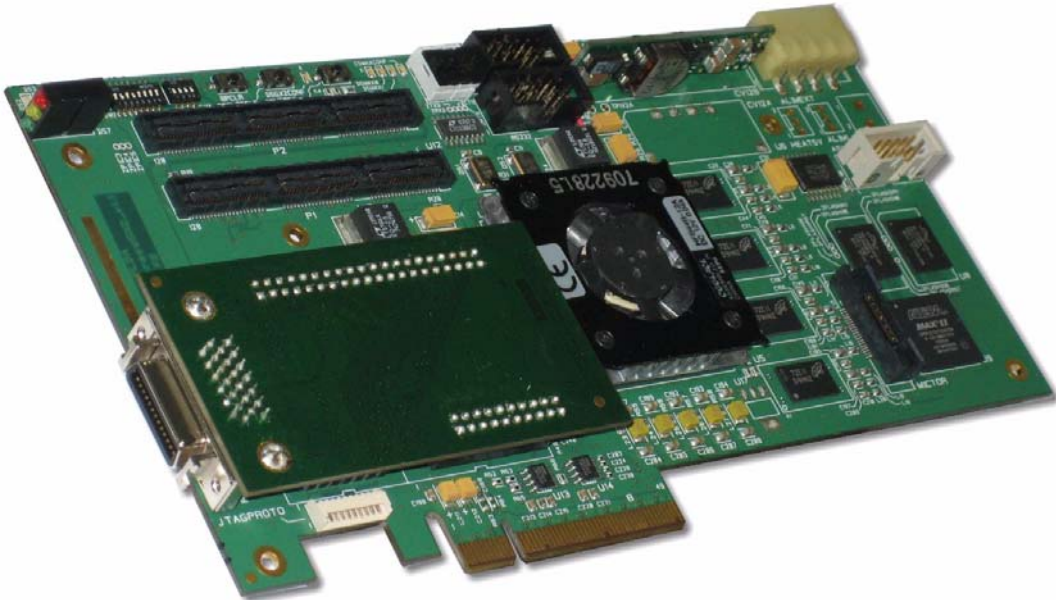


Figure 4: KLINK\_Base mounted on the XpressGXII

### 4.2 Mounting the KLINK\_Base on the XpressLXT

The following figure shows the KLINK\_Base daughter card mounted on the XpressLXT:

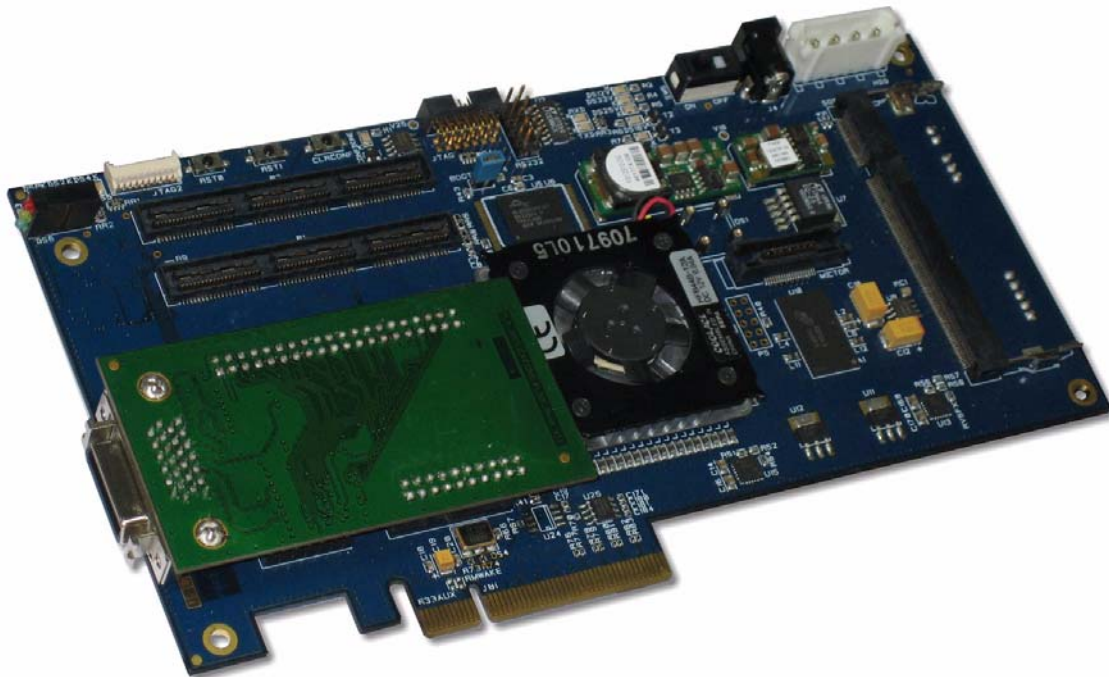


Figure 5: KLINK\_Base mounted on the XpressLXT

## 4.3 Mounting the KLINK\_Base on the XpressAGX

The following figure shows the KLINK\_Base daughter card mounted on the XpressAGX:

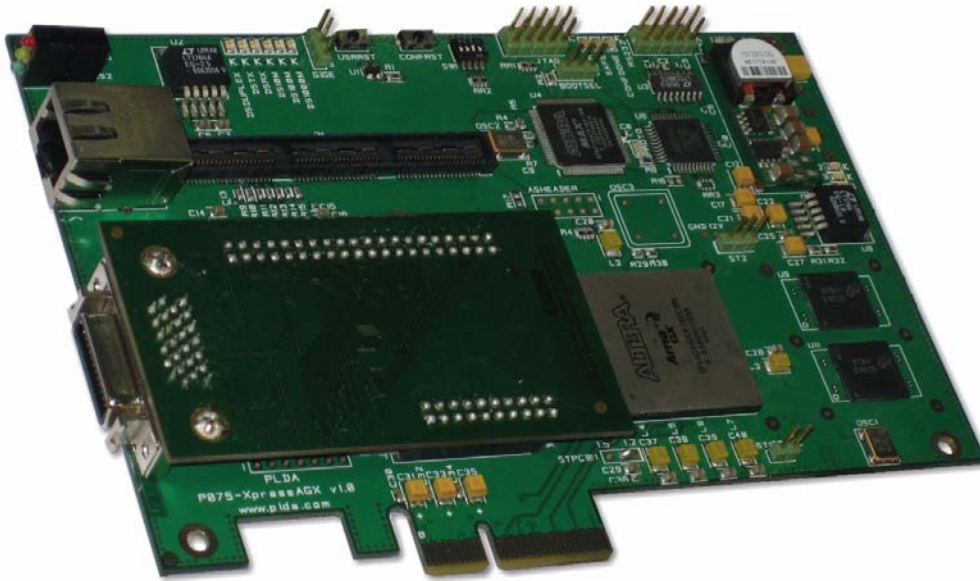


Figure 6: KLINK\_Base mounted on the XpressAGX

## 4.4 Mounting the KLINK\_Base on the XpressV5LC

The following figure shows the KLINK\_Base daughter card mounted on the XpressV5LC:

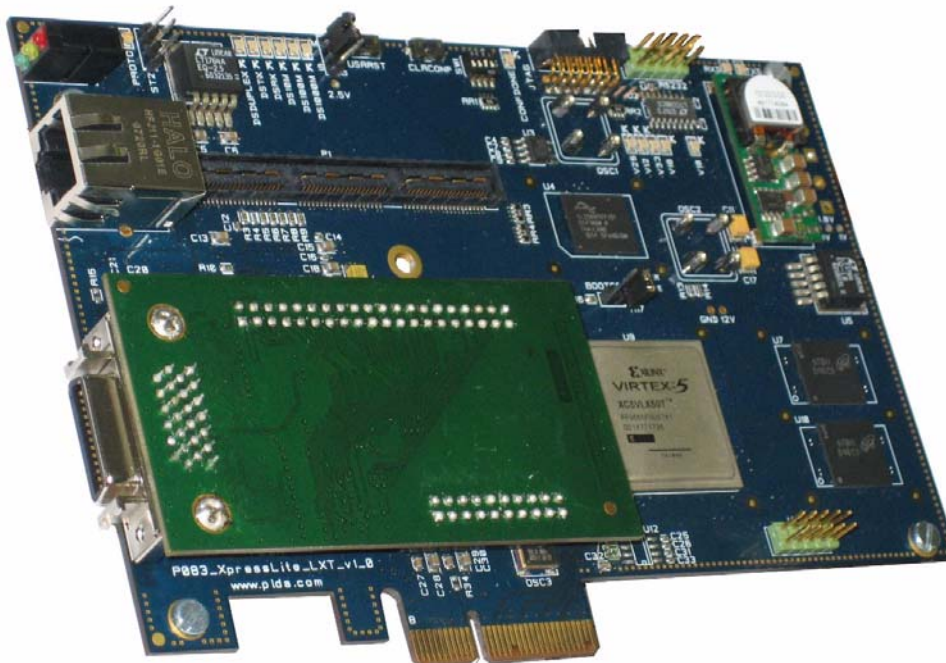


Figure 7: KLINK\_Base mounted on the XpressV5LC