

EZDMA

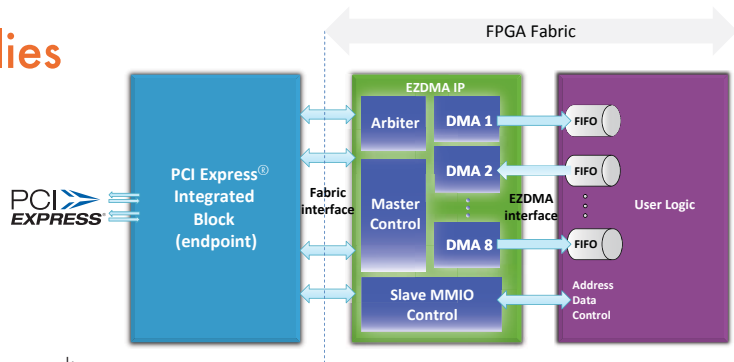
High-performance DMA



DMA Controller for Xilinx's PCI Express® v1.1 Integrated Block

Supported Families

- Virtex-6 LXT/SXT
- Virtex-5 LXT/SXT/FXT/TXT
- Spartan-6 LXT



Features

- PCI Express® v1.1 (Gen1) compliant
- Supports x1, x4, x8 lane configurations
 - Spartan-6 : x1, x2, x4
- 1 to 8 DMA channels
- Host-based scatter-gather support per channel
- DMA transfer size up to 4 GB per channel
- Up to 8 simultaneous read requests
- Integrated arbiter with round robin algorithm
- Address/data/control port for MMIO accesses
- Legacy and Native Power Management support
- Up to 32 MSI messages with 64-bit addressing

Deliverables

- Encrypted RTL or source code
- Customization GUI Wizard
- Simulation models
- Testbench (libraries)
- Endpoint reference design/DMA throughput demo
- PLDA Device Driver and SDK (Windows/Linux)
- Documentation
- Technical support

Benefits

- Shortens design cycles by hiding the complexity and limitations of Hard PCIe block fabric interfaces
- Higher performance than SoC based DMA engines
- Vendor-agnostic user interface allows seamless device migration
- Allows easy migration of designs using PLDA's PCI and PCI-X IP
- Allows easy migration of designs using PLDA's PCI Express® Soft-IP for FPGA (XpressLite and XpressLite2)
- Configurable for resource optimization
- Customizable to fit specific customer requirements
- Hardware proven IP, deployed in 400+ designs

Free Evaluation

- Same deliverables as licensed IP
- Evaluation period includes full access to technical support
- Request evaluation at www.plda.com/request_ip.php

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